ZERO DEFECTS

Entegris Newsletter

March 2015

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Entegris Receives Intel's Preferred Quality Supplier Award

Entegris, Inc. has been recognized as one of 19 companies receiving Intel Corporation's Preferred Quality Supplier (PQS) award for their performance in 2014. This supplier has demonstrated industry-leading commitment across all critical focus areas on which they are measured: quality, cost, availability, technology, customer service, labor and ethics systems and environmental sustainability. Entegris, Inc. is recognized for their significant contributions providing Intel with contamination control, critical materials handling, and advanced process materials, deemed essential to Intel's success.

"*We are truly honored to receive Intel's Preferred Quality Supplier award*," said Bertrand Loy, president and CEO of Entegris. "*This distinction is the result of the on-going commitment and dedication of the Entegris teams around the world to relentlessly advance our quality systems and our technology. We are committed to helping the world's technology leaders grow in an environmentally and socially responsible manner and we look forward to new opportunities to enable Intel's technology roadmap.*"

"*Congratulations to Entegris for winning the 2014 Preferred Supplier Quality Award! Entegris is a key supplier supporting Intel's wafer carriers and filtration technology requirements. Intel recognizes Entegris' dedication in providing excellent performances across Cost, Quality, Availability, Technology and Sustainability. We are looking forward to Entegris' continuing success and partnership in 2015*," said Tim Hendry Intel VP and Director of Fab Materials Operations, Intel Corporation.

The PQS award is part of Intel's Supplier Continuous Quality Improvement (SCQI) program that encourages suppliers to strive for excellence and continuous improvement. To qualify for PQS status, suppliers must score 80 percent on a report card that assesses performance and ability to meet cost, quality, availability, technology, environmental, social and governance goals. Suppliers must also achieve 80 percent or greater on a challenging improvement plan and demonstrate solid quality and business systems.

>> Additional information about the SCQI program is available at http://intel.com/go/quality.

Entegris at SPIE® Conference

Entegris recently participated at the 2015 SPIE® Advanced Lithography Conference (AL) in San Jose, California where we showcased our latest lithography technologies and shared the results of collaborative work with several industry leaders, including Tokyo Electron (TEL®), IMEC®, SCREEN, JSR® Micro, KLA-Tencor® and AZ Electronic Materials.

- A comprehensive approach for micro and multiple bridge mitigation in immersion photolithography
- Point-of-use filtration strategy for negative tone developer in extended immersion and extreme ultraviolet (EUV) lithography
- Defect mitigation and root cause studies in imec's 14 nm half-pitch chemo-epitaxy DSA flow

>> Learn more about wafer handling, filtration and packaging technologies featured at the show.

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Publisher: Entegris North America
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Entegris
creating a material advantage

Innovation

New Contactless Horizontal Wafer Shipper Family Offers Innovation Coupled with Increased Yields

By Doug Moser, Product Manager | Microenvironments | Finished Wafer/Backend - Entegris, Inc. and
Jorgen Lundgren, Senior Field Application Engineer – Entegris Europe

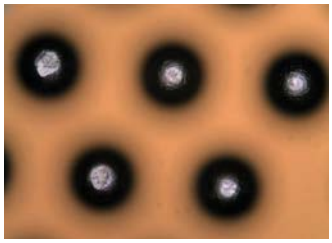
With wafer thicknesses decreasing to 150 µm and below, manufacturing challenges arise. Ultrathin wafers are less stable and more vulnerable to stresses, and the die can be prone to breaking and warping.

As technology is shifting to thinner and more sensitive wafers, many customers have expressed the need for a horizontal wafer shipper that enables them to:

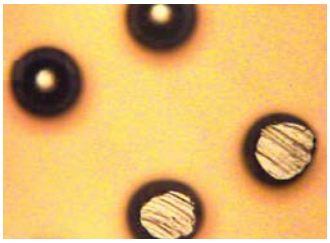
- **Protect their valuable wafers in an Electro Static Dissipative (ESD)** wafer shipping box.
- **Ship and store their most sensitive thinned, lens/bumped wafers** (LED, 3D wafers , MEMS, and Taiko) without damage or defects.
- **Eliminate yield losses** caused by current TYVEK® inserts and foam cushions.

Improvements vs. Standard HWS

Shipping this type of sensitive wafer in a traditional HWS can damage the wafer causing rejection as a result of deformed bumps or scratches. Lead bumps can be flattened or sheared in traditional HWS solutions with Tyvek interleaves.



Flattened



Sheared

In the contactless solution designed by Entegris, lead bumps are not in contact with any surface. **Contactless HWS avoids yield loss** due to wafer staining associated with TYVEK inserts.

Entegris Contactless Solution Benefits

The new Contactless HWS Family –150 mm, 200 mm and 300 mm, the HWS300C available in Q2 2015 – addresses the need for solutions to ship lens/bumped wafers.

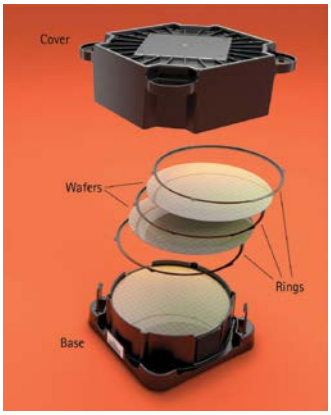
- **Lower cost due to less components** to order and inventory (TYVEK inserts/pink foam cushions)

200 mm Contactless Horizontal Wafer Shipper

- **Improved shipping density**
- **Improved lead time:** 3 – 4 weeks vs. current 16 weeks for TYVEK and pink cushion inserts
- **Better quality control:** Quality issues with the current TYVEK and pink cushion inserts (dimensional issues, ionic contamination, wafer stains, etc.)
- **No chemical contamination** and mechanical surface contact on the wafer
- Designed for **auto-compatibility**.

Product Overview

- Electro Static Dissipative (ESD) protective wafer shipping solution
- Wafers are placed on rings
- Rings keep the wafers from contacting each other
- Design eliminates the need to use TYVEK separators and pink foam cushions
- Designed for automatic compatibility



Performance Data

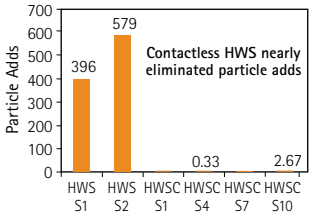
Minimum/Maximum Wafer Thickness

Product	Minimum Tested	Maximum Accommodated
HWS150C	150 µm	950 µm
HWS200C	150 µm	1100 µm
HWS300C	150 µm	1100 µm

ISTA-2A Drop Testing Performance (38"x10 Drops)

Product	Contents	Single Pack	Quad Pack
HWS150C	25 x 150 µm Si	PASS	PASS
HWS150C	25 x 675 µm Si	PASS	PASS
HWS200C	25 x 150 µm Si	PASS	PASS
HWS200C	25 x 725 µm Si	PASS	PASS
HWS300C	25 x 150 µm Si	PASS	Not Tested
HWS300C	25 x 775 µm Si	PASS	Not Tested

Particle Adds Comparison (All Sizes)



- *Testing with standard thickness wafers conducted at external laboratory*
- *Testing with thin wafers conducted at Entegris internal laboratory*
- *Testing of HWS300C product based on prototypes*

Test comparing 200 mm standard HWS (Tyvek/Foam) to Contactless HWS. HWS was loaded, vacuum bagged, unloaded. SP1 wafer scans of particles >0.12 µm

Innovation

Use of Entegris Purged FOUPs to Improve H-Terminated Silicon Surface Stability prior to Epitaxial Growth

By Kurt Wostyn, imec — Belgium

The surface cleanliness has a significant impact on the epitaxial process of a semiconductor. In the case of hetero-epitaxial growth of $Si_{1-x}Ge_x$ (SiGe) layers on Si in particular, the presence of oxygen has a substantial effect on the SiGe quality. Clean Si starting surfaces can be obtained by a high temperature H_2-bake (T >800°C). However, high temperature bakes can lead to undesirable roughening, relaxation of strained layers and can impact the integrity of small structures through surface reflow. In this paper we report on the **use of a N_2-purged Front Opening Unified Pod (FOUP)** to suppress the re-oxidation of Si surfaces after the pre-epi clean. The learnings are applicable to other pre-epi treatments.

Experimental

N_2-purging was evaluated using a modified Entegris A300 EBM FOUP featuring two snorkels at the back of the FOUP to uniformly distribute N_2. The Entegris Barrier Material (EBM) was used in the casing to further reduce diffusion of water vapor into the FOUP. An A300 poly(ether imide) (PEI) FOUP without N_2-purging was used as reference.

H-terminated surfaces were created by applying a high temperature bake (T = 1050°C) in a conventional ASM Epsilon® 3200 epi reactor. The re-oxidation of the Si surface was studied by exposure of the H-terminated surface to different environments. Further re-oxidation of the H-terminated Si surface between the test and analysis was prevented by capping the surface with an epitaxial 80nm Si-cap/80nm $Si_{0.8}Ge_{0.2}$ bilayer. The surface re-oxidation has been quantified directly by SIMS (Secondary Ion Mass Spectrometry) and indirectly by surface light scattering using a KLA-Tencor® Surfscan SP3.

Results and Discussion

The re-oxidation of H-terminated Si was evaluated at the center of the wafer by SIMS (Fig. 1). The graph compares the interfacial oxygen concentration after $Si_{0.8}Ge_{0.}$ epitaxy and with exposure of the 1050°C H_2 baked surface to different ambient conditions: (1) N_2-purged load lock (30 min); (2) storage inside a docked non-purged FOUP (1 hr); and finally (3) storage inside a N_2-purged FOUP (1 hr).

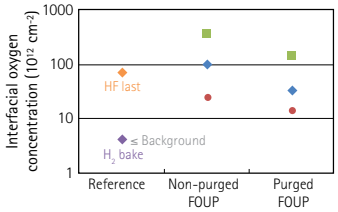


Figure 1: Interfacial oxygen concentration measured by SIMS between Si substrate and the epitaxial 80 nm Si-cap/80 nm $Si_{0.8}Ge_{0.2}$ bilayer grown on a 300 mm Si substrate. Values were measured at 3 positions: north (square), center (diamond), and south (round).

Exposure of the H_2-baked wafer to the N_2-purged load-lock for 30 min shows an oxygen concentration below the background signal of SIMS at the epitaxial-SiGe/Si-substrate interface. The purged FOUP shows a lower interfacial oxygen concentration (factor of ~ 4) at the center, north and south of the wafer compared to the standard FOUP.

Oxygen at the interface between the Si substrate and epitaxial $Si_{0.8}Ge_0$ enhances slippage along the {111} planes resulting in surface steps aligned in the <110> direction. An increase in misfit density will be observed by an increase in roughness of the epitaxial bilayer. Low-spatial-frequency light-scattering-intensity maps (called haze maps), were used to quantify these surface steps using the hazeline algorithm. The median haze and the range of haze values is significantly higher for the non-purged FOUP when compared to the load-lock reference and the purged FOUP, see Fig. 2. Exposure of the baked wafer to the purged FOUP leads to only a small increase in haze range while the median haze remains constant when compared to the load-lock reference.

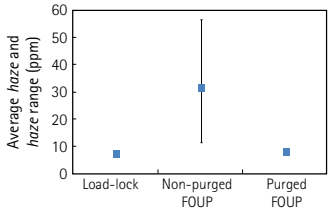


Figure 2: Median haze and haze range measured after the deposition of an epitaxial 80 nm Si-cap/80 nm $Si_{0.8}Ge_{0.2}$ bilayer for the expose of the H_2 baked wafer to different ambient conditions: load-lock, non-purged FOUP and N_2-purged FOUP.

The north-to-south non-uniformity in hazeline density correlates with the non-uniform re-oxidation of the surface measured by SIMS (see Fig. 1). The spatial dependent oxygen concentration for the purged FOUP indicates that an increase in N_2 flow can further reduce re-oxidation across the whole wafer surface. Some parts of the wafer at the south-east and south-west shows no or only a small increase in hazeline density compared to the load-lock reference, indicating that no or only a limited amount of re-oxidation occurred. This observation supports the feasibility of purged FOUPs to control the re-oxidation of H-terminated Si surfaces within an 1-hour time interval.

Conclusion

In this paper we report on the impact of queue time of an H-terminated Si surface in a non-purged PEI FOUP compared to a N_2-purged EBM FOUP. The interfacial degradation, as measured by SIMS and surface light scattering for 1 hour of queue time, is shown to be better controlled when using the N_2-purged EBM FOUP. Further optimization of the N_2 flow is needed to suppress re-oxidation of the H-terminated Si surface across the whole wafer surface. Although the procedure of a H_2-bake offers the most-controllable scheme for creating an H-passivated Si surface, the learnings are also applicable to wet-chemical pre-epi treatments.

This work has been published in ECS Transactions 64, 669-673 (2014).

Acknowledgements: K. Wostyn, D. Rondas, K. Kenis, R. Loo, A. Hikavyy, B. Douhard, P.W. Mertens, F. Holsteyns, S. De Gendt — imec vzw, Kapeldreef 75, 3001 Leuven, Belgium; L. D'Urzo, L. Van Autryve, R.R. Lieten — Entegris GmbH, Hugo-Junkers-Ring 5, 01109 Dresden, Germany.

Process Stability

Entegris Launches Dispense System Optimized for 3D and MEMS Applications

By Entegris, Inc.

Building on the proven performance of two-stage dispense technology, combined with Entegris' innovative Connectology® filter design, the IntelliGen® MV dispense system integrates **high-purity filtration with repeatable dispense of mid-viscosity fluids** (100–300 cP).

The integrated, dual-pressure sensor simplifies recipe programming and filter priming with user-friendly dispense diagnostics and **real-time alerts** in an intuitive programming interface. IntelliGen MV includes several diagnostic features (such as dispense confirmation, cycle time confirmation and ΔP confirmation) that notify when a partial or failed dispense occurs to help minimize costly wafer defects due to coating problems. The state-of-the- art air detection feature pinpoints when air enters the outlet tubing from a leak or from minute air bubble formations that gradually accumulate over time.

Real-time, interactive diagnostics and feedback

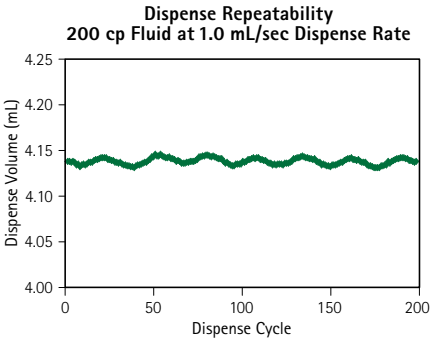
The compact design, superior performance and interactive diagnostics make IntelliGen MV dispense system the right choice to **ensure dispense repeatability, longer filter life and a greater return on investment**.

Features and Benefits

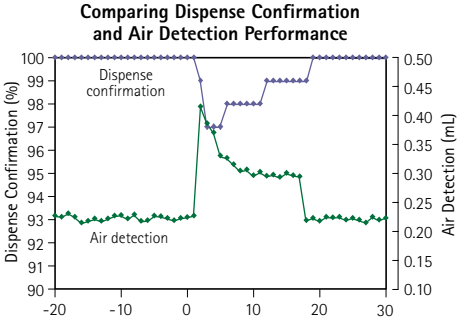
Two-stage dispense technology combined with Connectology filter design	Integrates high-purity filtration with repeatable dispense of mid-viscosity fluids (100 – 300 cP) • Impact® 2 V2 (OF style) filter slides into IntelliGen MV's compartment • Fluid passes through the Impact filter at the optimum flow rate for the specified retention rating
	Multiple dispense systems can fit into a single track to: • Process several chemistries simultaneously • Maximize filter performance even in the most sensitive photochemicals
Real-time, interactive diagnostics in intuitive programming interface	Simplifies recipe programming and filter priming
	Integrates dual-pressure sensor
	Provides user-friendly dispense diagnostics and real-time alerts • Several diagnostic features notify when a partial or failed dispense occurs to help minimize costly wafer defects due to coating problems • State-of-the-art air detection feature pinpoints when air enters the outlet tubing from a leak or from minute air bubble formations that gradually accumulate over time

Performance Data

The following graph shows dispense repeatability trending over a span of 200 dispense cycles.



The following graph compares dispense confirmation and air detection performance at a 300 cP chemical level when a 0.3 mL air bubble is introduced into the process.



Cost Reduction

Formulating a One-step, FEOL, post-CMP Cleaner to Maximize Process Efficiency and Reduce Cost

By Cuong Tran, Don Frye and Steve Medd – Entegris, Inc.

Changes to the number and types of films exposed during cleaning have highlighted a need for formulated cleans in the Front End of the Line (FEOL) process. In addition, changes to the particles used in slurries have rendered many of the traditional post-CMP (pCMP) commodity cleaners ineffective for this process. Ideally, this cleaning step should be a one-step process. These challenges are pushing companies to consider formulated cleans over commodity cleans. A formulated clean can remove particles and metal contamination all in one step, while protecting the underlying thin films. Here we summarize a path toward the development of this type of cleaner.

Our goal was to develop a pCMP cleaner formulation that had high efficiency for Ceria particle removal and no or very low etch rate on silicon oxide, silicon nitride, or silicon. Our requirements for demonstrating pCMP cleaning of Ceria particles were as follows:

1. No damage of silicon oxide, silicon nitride or silicon surfaces
2. High removal efficiency for Ceria particles
3. No metal impurities left on surface

As we raise the pH of the cleaner more $Ce(OH)_3$ will be formed as seen in Figure 1.

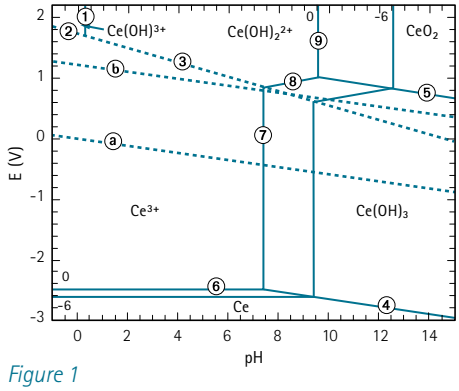


Figure 1

Figure 2 tells us that a higher pH will be needed to repel the Ceria particles from the surface for these older forms of Ceria.

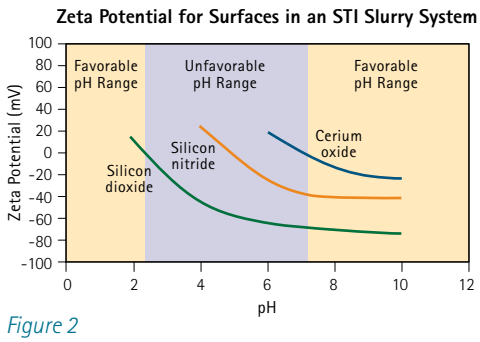


Figure 2

In addition to compatibility to the new thin films and removal of the new slurry particles, companies are finding that a formulated clean can simplify the cleaning process. Current cleans might involve a two-step process to remove the slurry residue after polish and the metal ion contamination which might remain after processing. However, a formulated clean can remove both in one-step. This can simplify the cleaning process and reduce the Cost of Ownership (COO).

Discovering the Way Forward

Etch rates were calculated by measuring each material's film thickness before and after a beaker dip in concentrated chemistry. Ellipsometry was used to measure film thickness for all materials other than copper. A four-point probe was used to measure copper film thickness change. Coupons for each film were dipped in each formulation for up to 60 minutes. In all cases, the film thickness change was within the measurement noise for the given method (zero etch rate).

Full wafer cleaning results were generated using a developmental Ceria slurry from a major supplier. Next, 200 mm blanket TEOS wafers were polished on an Applied Materials® Mirra® polisher and cleaned on an Ontrak Series II brush cleaner. Wafers were polished for 30 seconds on a DOW® IC1010™ pad to provide a fresh polished surface.

Cleaning formulations were diluted to their point-of-use concentrations (60:1) and were dispensed through the spray bar in both brush stations. A short cleaning time of 20 seconds was used in each brush station to exaggerate the defect count so chemistry performance could be more easily differentiated. A 20-second DI water rinse followed each chemistry step. Defect counts were generated using a KLA-Tencor® SP1.

Zeta potential and particle size measurements were performed using a Beckman Coulter® DelsaMax Pro tool. A Ceria slurry from a major supplier was diluted 1:10 with DI water to bring the solids content down into the instrument's detection range. The diluted slurry was then titrated with either a strong acid/base or one of our development formulations. The diluted slurry has a pH of 3.8. HCl and KOH were used as the strong acid/base titrants to create a pH range of 2 to 12. Development formulations B (pH 2.5) and C (pH 11) were also used to create a pH range of 3 to 10. Particle size and Zeta Potential measurements are carried out simultaneously by the instrument.

Tungsten slurry cleaning tests were performed using a silica-based tungsten slurry from a major supplier. Blanket TEOS wafers were polished for 60 seconds and then buffed with DI water for 60 seconds. They were then cleaned with the brushes in the open position for 15 seconds and rinsed with DI water for 15 seconds. Surface particles were analyzed by SEM.

continued on the next page

Cost Reduction

Our Legacy and Developmental cleans are all formulated products. All are high pH formulations, >9pH, except Developmental B which is <5 pH.

Results

In Figure 3 we see that this class of chemistries has very low etch rates for common thin films. All films have Etch Rates (ER) near 0. These chemistries do not seem to etch these thin films.

	Legacy A	Dev. A	Dev. B	Dev. C
Material	ER (A/min)	ER (A/min)	ER (A/min)	ER (A/min)
TiN	<0.1	<0.1		
TaN	<0.1	<0.1		
SOG	<0.1	<0.1		
P-SiN	<0.1	<0.1	<0.1	<0.1
HDP	<0.1	<0.1		
P-SiO2	<0.1	<0.1		
P-Silicon	<0.1	<0.1		
TEOS	<0.1	<0.1	<0.1	<0.1
Cu	<0.1	<0.1		

Figure 3

Figure 4 shows cleaners Legacy A and Development A illustrating good cleaning. Note normalized defects along the y axis. An SP1 is used to count defects. A defect count of 1 is our minimum requirement baseline.

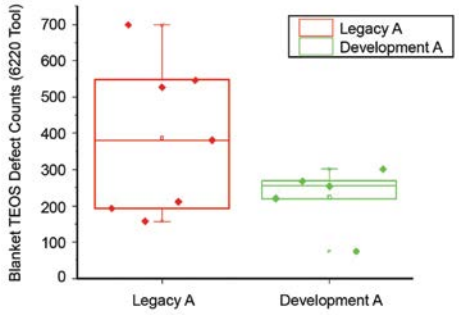


Figure 4

Figure 5 shows a TEOS surface with Ceria particles before and after clean by Legacy Cleaner A.

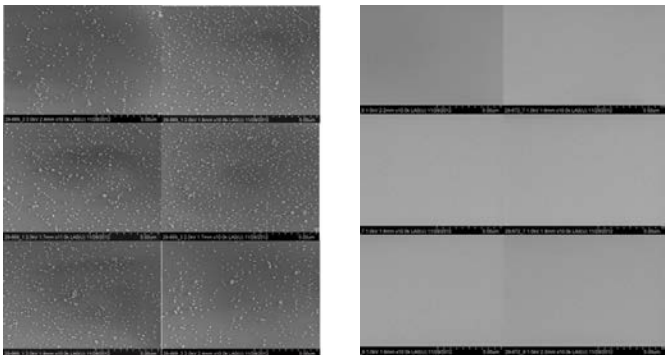


Figure 5: Ceria particles on surface *Cleaning by Legacy A (60:1)*

Conclusions

From Ceria to colloidal silica removal, formulated cleans can provide good cleaning at reduced complexity. **As the underlying structure becomes even more complex, as in a FinFet structure, the formulated cleans will reduce the loss of under-lying thin films, making the structure easier to build and yielding higher performance with the use of thinner films. Moving to a single-step clean will improve yield and reduce the tool footprints in the fab.** We have shown that formulated cleans can remove Ceria and silica particles from nitride and TEOS films and identify a path to develop a new class of cleaners giving even higher performance.

Product Highlight

Torrento® X Series High-Flux Filters: Enable Breakthrough Particle Protection and Unsurpassed Cleanliness

Torrento X series filters facilitate "drop-in replacement" of new or existing filters and meet the critical customer demands at advanced wet, etch and clean technology nodes.

Superior Particle Protection

Torrento X series filters utilize an applications-optimized, high-flux membrane that delivers a high flow rate and low pressure drop for its performance rating. This reliable, field-proven, nondewetting membrane technology achieves superior particle protection in advanced semiconductor fabs, and enables precise, yield-enabling filtration in sub-24 nm device geometry applications.

Ultra Cleanliness

Torrento X series filters come standard with the Entegris ultra-low metallic cleanliness technology (UCM), removing the most challenging contaminants in advanced processes and enhancing startup time. Entegris also offers an Extreme UCM option (XUCM) for higher level cleanliness needs and faster startup times.

Operational Efficiencies

Torrento X series cartridge and disposable filters enable greater installation flexibility, reduce equipment retrofits required for node transition, extend filter lifetime, and ultimately cut overall operational costs. The disposable design eliminates operator handling of the filter element and enables configuration continuity.

Features	Benefits
Superior particle protection	Yield enabling at smaller geometries
	Reliable, field-proven, nondewetting membrane technology
Ultra cleanliness	Comes standard with Entegris ultra-low metallic cleanliness technology (UCM) • Ensures ultra cleanliness • Enhances startup time Extreme UCM (XUCM) option available for higher cleanliness needs and faster startup times
Operational efficiencies	Enables greater installation flexibility • Reduces equipment retrofits required for node transition • Extends filter lifetime • Cuts overall operational costs
	Disposable design • Eliminates operator handling of the filter element • Enables configuration continuity
Aqueous-based chemical compatibility	Recommended for ambient and elevated temperatures including H_2SO_4, H_3PO_4, HNO_3, HCl, NH_4OH, H_2O_2, SC2 and various strippers

Feedback

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